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A NEW SUGGESTION OF REAL NETWORK-CONNECTED CONVERTER FOR COMMON MODE CURRENT DIMINUTION IN PHOTOVOLTAIC (PV) TRANSFORMERLESS SYSTEMS

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ABSTRACT

The conventional network-connected photovoltaic inverter includes either a line frequency or a high frequency transformer between the inverter and grid. Many transformerless topologies for photovoltaic (PV) systems were planned in order to diminish power losses and avoid high levels of common-mode current. In household network connected PV applications a single phase converter is typically used. The abolition of the output transformer from network-connected PV systems not only reduces the cost, mass, and weight of the conversion stage but also increases the system overall efficiency. The model of a photovoltaic (PV) network-connected converter usually comprehends a galvanic isolation between the network and the PV panels. Recently, in low power systems, the galvanic segregation has been separated with the aim to increase efficiency and reduce the cost of the converter. Due to the of a stray capacitance between the PV panel, usually connected to earth, a high value of common mode current (i.e., ground leakage current) can arise. While protection requirements in transformer less systems can be met by means of outside elements, common-mode current and the vaccination of direct current (dc) into the network must be assured topologically or by the inverter's control system. In order to bind the common mode current, new converter topologies have been planned. Amplitude and spectrum of the soil current depends upon the converter topology, the switching strategy, and the resonant circuit formed by the soil capacitance (stray capacitance), the converter, the ac filter, and the network. Experimental and matlab simulation result confirm the effectiveness of the planned solution.

KEYWORDS: Common-Mode Current, Junction Capacitance, PV Systems, Sinusoidal Pulse Width Modulation (SPWM) Strategy, Transformerless Inverter

INTRODUCTION

In network-connected, low-power PV plants, a plants, a single phase converter is used to make simpler network connection a line transformer or a high-frequency transformer is typically present in its architecture. Recently, with the aim of minimizing power losses and cost, many researchers investigated the possibility of removing the transformers and a few transformers less topologies have been proposed for network-connected power converters [1],[2].

In single phase topology the full bridge is widely used. This topology allows bipolar or unipolar PWM modulation. From fig.1 the common-mode voltage result during a switching cycle in case of unipolar PWM is computed in this section [4].In a full bridge converter, the common mode current can be controlled by imposing a constant common mode voltage Vcm, defined as $v_{cm} = \frac{v_{AO} + v_{BO}}{2}$ (See fig.1, where the reference potential is the low side of the dc bus), at the converter output [3].

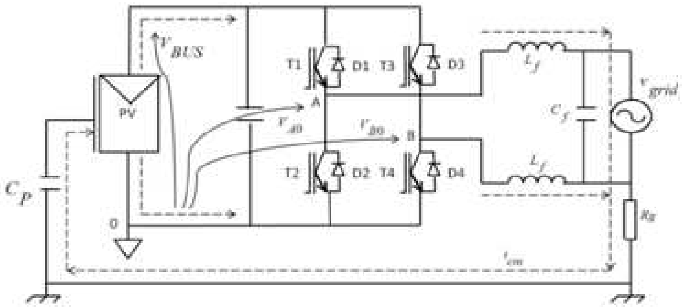

Figure 1: Full-Bridge Inverter with PV DC Source [4]

This is made to positive output voltage and current (first quadrant operations); output voltage is as $v_{AB} = v_{AO} - v_{BO}$. The switching cycle consists of four possible configurations:

T1, T4 On (T2 and T3 Off): $v_{AB} = V_{BUS}$, $v_{cm} = \frac{V_{BUS}}{2}$.

T2, T4, D2 On: $v_{AB} = 0$. Low side current freewheeling through D2, T4, $v_{cm} = 0$

T1, T4 On (T2 and T3 Off): $v_{AB} = V_{BUS}$, $v_{cm} = \frac{V_{BUS}}{2}$.

T1, T3, D3 On: $v_{AB} = 0$. High side current freewheeling through T1, D3, $v_{cm} = V_{BUS}$.

The common mode voltage v_{cm} varies from 0 to V_{BUS} and a large ground leakage current will flow.

COMPENSATION OF ASYMMETRIC COMMUTATION FOR UNIPOLAR TRANFORMERLESS (UNITL) INVERTER

- Basic idea able to solve this problem are shown in fig.2, which two additional blocks are added named DC Decoupling block, which limits the common mode voltage to $V_{BUS}/2$ value.
- The DC decoupling blocks disconnect the full bridge from DC Source during the current freewheeling. During low side freewheeling T6 is switched off while during high side freewheeling T5 is switched off [5, 6].

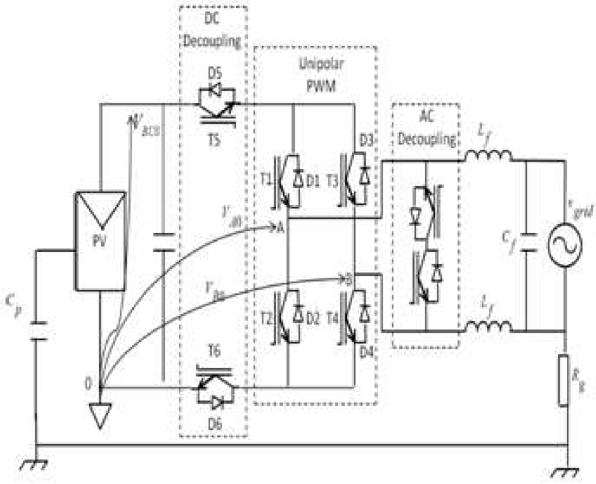

Figure 2: UniTL Topology [5]

The PWM switching strategy is shown in Fig.3, where signals of the standard unipolar PWM are x and y.

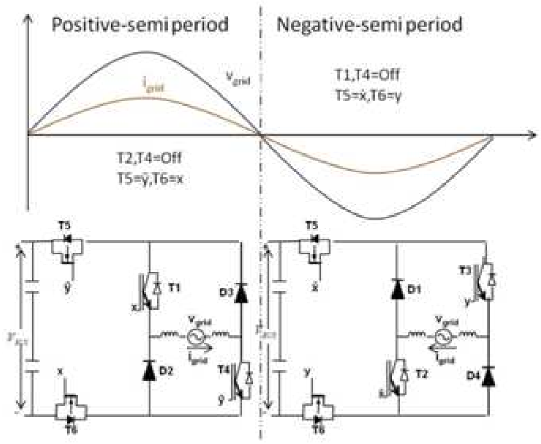

Figure 3: UniTL Modulation Switching Scheme [4]

In order to improve the efficiency, converter must inject current into the grid with a unity power factor. During the high-side freewheeling phase, the injected grid current is flows through T1 and D3) T5 is OFF and the voltage at the high-side of the full-bridge, in ideal conditions, equals $V_{BUS}/2$Similarly, during the low-side freewheeling, T6 is OFF and the voltage at the low-side of the full-bridge, in ideal conditions, equals $V_{BUS}/2$ [6].

SIMULATION RESULTS

For the simulation of Single phase inverter with DC decoupling the simulation parameters are use as in shown in Table 1.

Table 1: Simulation Parameters of Full Bridge Inverter

Bus Voltage	V_{BUS} = 400V
Grid voltage	V_{grid} = 230V_{rms}
Grid frequency	f=50Hz
Ground to neutral resistance	R_{ground} = 2ohm
PV parasiticcapacitance	C_{PV} = 14nF
Inductor output filter	L_f = 2mH

Table 1: Contd.,	
Capacitor output filter	C_f = 2.2□F
Passive damping resistance	R_f = 0.5 ohm
Grid inductance	L_{grid} = 40□H
Switching frequency	f_{sw} = 10kHz
DC link Capacitor (calculated)	C=4mF

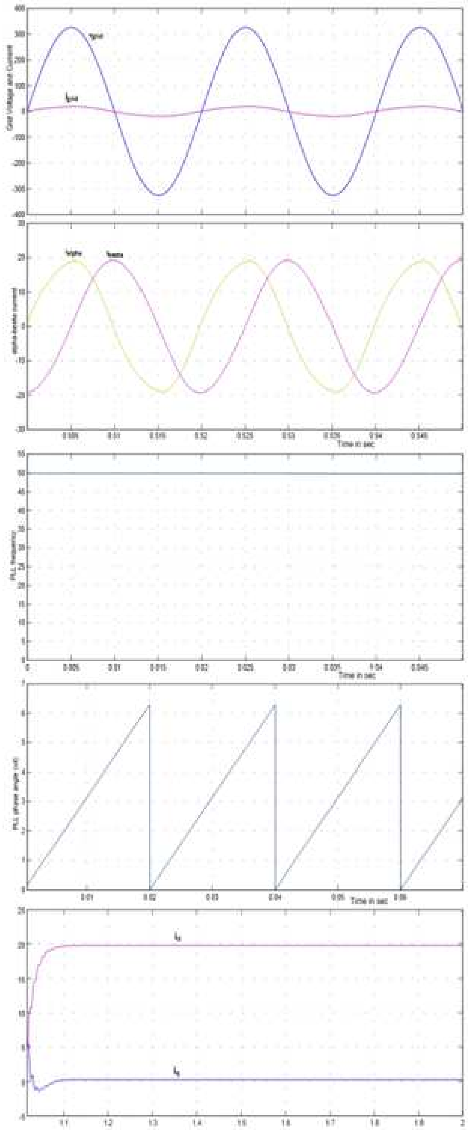

Figure 4: Simulation Results (A) Grid Voltage and Grid Current (B) Stationary Frame Component of Grid Current (C) Grid Frequency (D) Grid Phase Angle (E) Synchronously Rotating Frame of Grid Current

From simulation result we can see that the grid voltage and grid current are in phase and phase angle in locked. In order to improve the efficiency, the converter must inject current into the grid with a unity power factor.

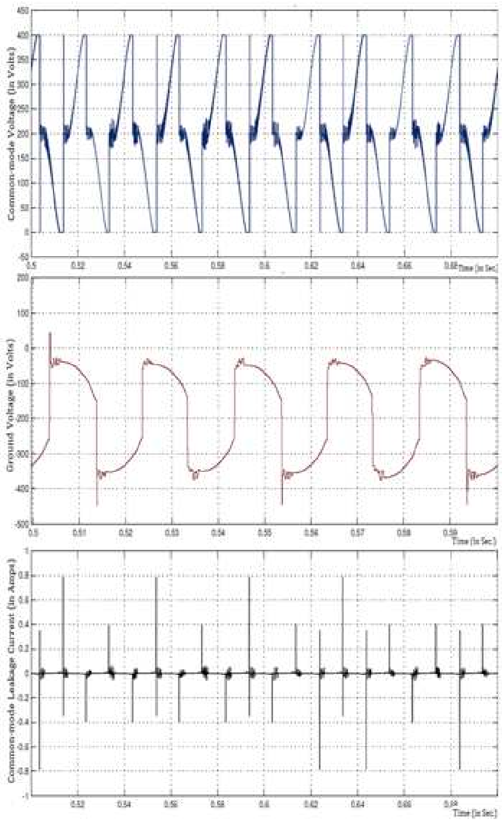

Figure 5: Simulation Results of (a) Common-Mode Voltage (b) Ground Voltage (c) Common-Mode Leakage Current

Simulation results show that a small asymmetry in the switching circuit would lead to strong variation of v_{cm}, up to V_{BUS} (i.e. 400 volt.), as a consequence the ground voltage v_{ground} contain high frequency components with the fundamental grid frequency (Fig. 2.1 (c)). The resulting common-mode leakage current is very large variation about 0.8A, as shown by Fig. 2.2 (c). Hence the variation of common-mode voltage is same as of a conventional full-bridge inverter driven by unipolar PWM [4]. So common-mode leakage current also increases and asymmetry caused common mode leakage current with maximum variation magnitude is 0.8A at any instant.

Therefore it is necessary to reduce common mode voltage variation, as a result of this common mode leakage current automatically reduce.

ADDITIONAL CLAMPING DIODES TO REDUCE COMMON MODE VOLTAGE VARIATIONS FOR UNIPOLAR TRANSFORMERLESS INVERTER

Common mode voltage variations reduction due to asymmetric commutations is takes place only during freewheeling phases, is realized by adding two additional low power switches which clamp the high or the low sides of the full-bridge. In order to avoid the complexity which introduced by two controlled switches so two diodes are used instead of power switch [4, 7].

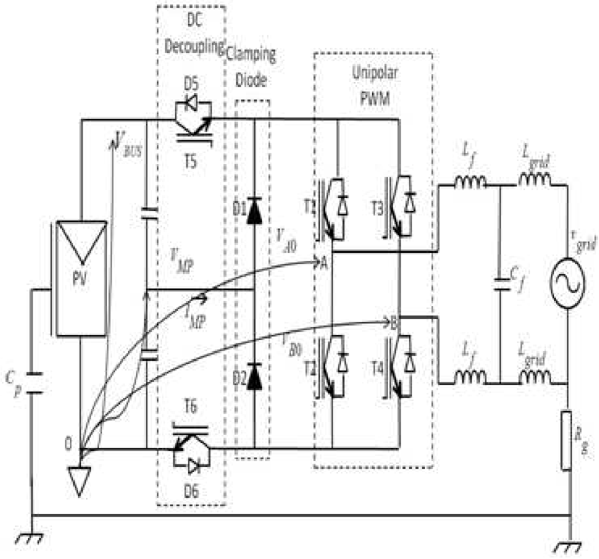

Figure 6: UniTL Topology with Clamping Diode [7]

From figure we see that the clamping diode D1 and D2 are added. Therefore both high side and low side of full bridge are floating to the midpoint voltage V_{MP} due to parasitic capacitances; starts to decrease but the inserted diode will clamp it to $V_{BUS}/2$.

PWM switching strategy is shown in figure below, where x and y are standard unipolar PWM signals.

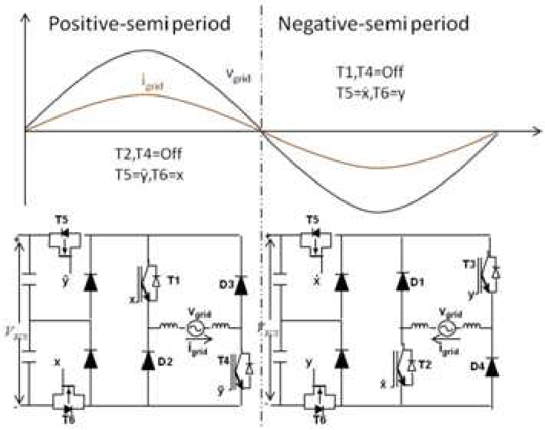

Figure 7: PWM Control Strategy for Every Semi-Period

With above figure we can say that in first quadrant operations (positive output voltage and current) the following sequential configurations are possible in a switching cycle:

T1, T4, T5, T6 ON: $v_{AB} = V_{DC}, v_{cm} = \frac{V_{BUS}}{2}$.

T2, T4, T5, D2 ON: $v_{AB} = 0$. Low side current freewheeling through T4, D4: $v_{cm} = V_{A0} = V_{B0} = \frac{V_{BUS}}{2}$.

T1, T4, T5, T6 ON: $v_{AB} = V_{DC}$, $v_{cm} = \frac{V_{BUS}}{2}$.

T1, T3, T6, D3 ON: $v_{AB} = 0$. High side current freewheeling through T1, D3: $v_{cm} = V_{A0} = V_{B0} = \frac{V_{BUS}}{2}$.

The common mode voltage v_{cm} is locked to $V_{BUS}/2$ and ground leakage current reduces.

SIMULATION RESULTS

For the simulation of Single phase inverter with DC decoupling and clamping diode the simulation parameters are use as in shown in Table 1.

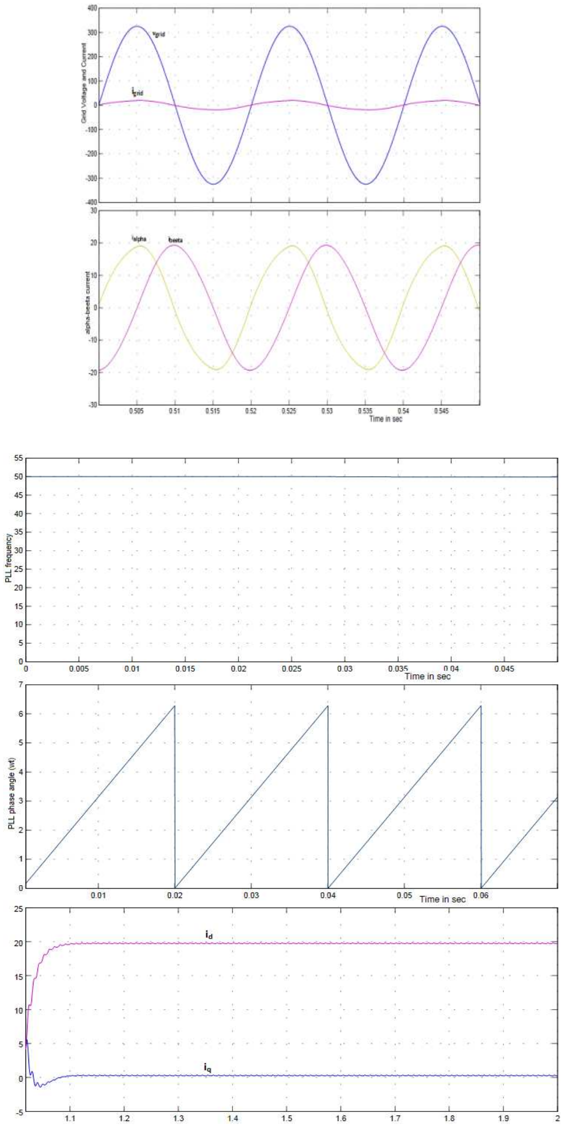

Figure 8: Simulation Results (a) Grid Voltage and Grid Current (b) Stationary Frame Component of Grid Current (c) Grid Frequency (d) Grid Phase Angle (e) Synchronously Rotating Frame of Grid Current

From simulation result we can see that the grid voltage and grid current are in phase and phase angle in locked. In order to improve the efficiency, the converter must inject current into the grid with a unity power factor.

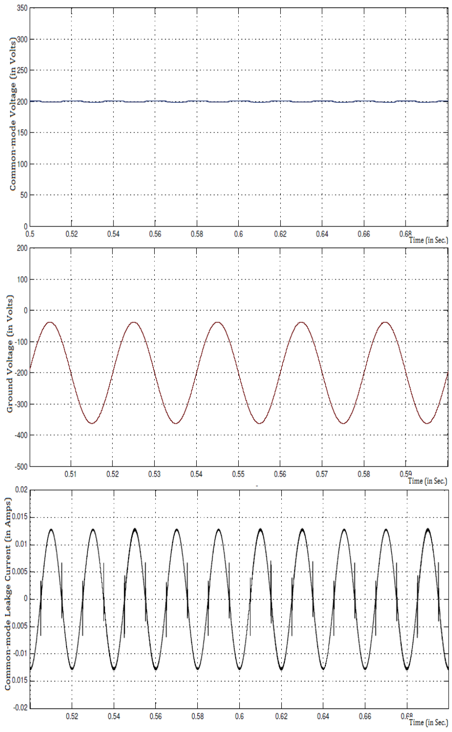

Figure 9: Simulation results (a) Common-Mode Voltage (b) Ground Voltage (c) Common-Mode Leakage Current

Also simulation results confirm the hypothesis. The two diodes impose a maximum voltage equal to $V_{BUS}/2$ across T5 and T6 when they are off. Nevertheless the performances of this simple solution are affected by the value of the PCB parasitic capacitances and inductances.

Simulation result also show the common mode voltage v_{cm} is locked to as a $V_{BUS}/2$; consequence the ground voltage v_{ground} doesn't contain high frequency components and only the fundamental grid frequency is present (Figure. 3.1 (C)). The resulting common-mode ground leakage current is very small 13mA, as shown by Fig. 3.2 (C).

CONCLUSIONS

Several transformerless topologies are studied and simulated in term of common mode voltage, ground voltage and leakage current. In dissertation a feasible solution to reduce ground leakage current in transformerless full bridge converter driven by unipolar PWM is described and simulated. It relies on two suitable blocks added to a typical full bridge converter scheme: the DC decoupling block and the clamping diode with the aim to lock the common mode voltage to VDC/2.

REFERENCES

1. Lopez, Oscar; Teodorescu, Remus; Freijedo, Francisco; DovalGandoy, Jesus; "Leakage current evaluation of a singlephase transformerless PV inverter connected to the grid," Applied Power Electronics Conference, APEC

2007–Twenty Second Annual IEEE feb. 25 2007-March 1 2007 Page (s):907-912.

2. Gonzalez, R.; Lopez, J.; Sanchis, P.; Marroyo, L.; “Transformerless Inverter for Single-Phase Photovoltaic Systems” Power Electronics, IEEE Trans. On Volume22, Issue 2, March 2007, Page (s):693-697.
3. G.Buticchi, D.Barater, E. Lorenzani, and Giovanni, “Digital control of actual grid-connected converters for ground leakage current reduction in PV transformerless systems,” IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS, VOL.8, NO.3, PP.563-572, AUGUST 2012.
4. D. Barater, G. Buticchi, A. S. Crinto, G. Franceschini, and E. Lorenzani, “A new proposal for ground leakage current reduction in transformerless grid-connected converters for photovoltaic plants,” in *Proc. 35th Annual Conf. IEEE Ind. Electron. Soc., IECON’09*, Porto, Portugal, Nov. 20, pp. 4567–4572.
5. E-Habrouk M., Darwish M.K., Mehta P., "Active power filters: a review", IEEE Proceedings-Electric Power Applications, Vol. 147, Iss.5, pp. 403-413, 2000.
6. S. V. Araujo, P. Zacharias, and R. Mallwitz, “Highly efficient single phase transformerless inverters for grid-connected photovoltaic systems,” *IEEE Trans. Ind. Electronic*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010.
7. R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, “Transformerless inverter for single-phase photovoltaic systems,” IEEE Trans. Power Electron., vol. 22, no. 2, pp. 693–697, Mar. 2007.
8. Oscar Lopez, Francisco D.Freijedo, Alejandro G.yepes, Pablo Fernandez-Comesana, Jano Malvar, Remus Teodorescu, Jesus Doval-Gandoy, “Eliminating ground current in a transformerless photovoltaic application,” IEEE TRANS. ON ENERGY CONVERSION,VOL. 25, NO. 1, pp.140-147, MARCH 2010.
9. V. Abinaya, B.Prabakaran, R.B.Selvakumar, “An improved transformerless inverter for grid-connected photovoltaic power system,” International Journal of Engineering and Innovative Technology (IJEIT), Volume 2, Issue 12, pp.5-9, June 2013.
10. D.Barater, G. Buticchi, E.Lorenzani, V.Malori, “Transformerless grid-connected converter for pv plants with constant common mode voltage and arbitrary power factor,” in proc. IEEE Industrial Electronics Society IECON 2012-38th, annual IEEE 2012, pp. 5756-5761.
11. Roberto Gonzalez, Eugenio Gubia, Jesus Lopez, Luis Marroyo, “Transformerless single-phase Multilevel-based photovoltaic inverter,” IEEE TRANS. ON INDUSTRIAL ELECTRONICS, VOL.55, NO.7, JULY 2008,pp.2694-2702
12. Bo Yang, Wuhua Li, Yunjie Gu, Wenfeng Cui, Xiangning He “Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a photovoltaic Grid Connected Power system,” IEEE Transactions on Power Electronics, vol.27, no.2,February 2012
13. Huafeng H. Xiao and S. Xie, “Leakage current analytical model and application in single-phase transformer less photovoltaic grid connected inverter,” IEEE Trans. Electromagn. Compat., vol. 52, no. 4, pp. 902–913, Nov. 2010.

14. T. Kerekes, R. Teodorescu, P. Ro-driguez, G. Vanquez, E.Aldabas, “A new high efficiency single phase transformerless Inverter topology”IEEE Transaction on industrial electronics, vol.58, no.1, jan 2011

15. R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, “Transformer less inverter for single-phase photovoltaic systems, ” IEEE Trans. Power Electron.,vol. 22, no. 2, pp. 693–697, Mar. 2007

16. G. Vazquez, T. Kerekes, A. Rolan, D. Aguilar, A. Luna, and G. Azevedo, “Losses and CMV evaluation in transformer less gridconnected PV topologies,” in Proc. IEEE Int. Symp. Ind. Electron., Jul. 2009, pp. 544–548.

17. T. Kerekes, R. Teodorescu, and U. Borup, “ Transformerless Photovoltaic inverters connected to the grid,” in Proc. IEEE 22nd Annu. Appl. Power Electron. Conf., 2007, pp. 1733–1737.